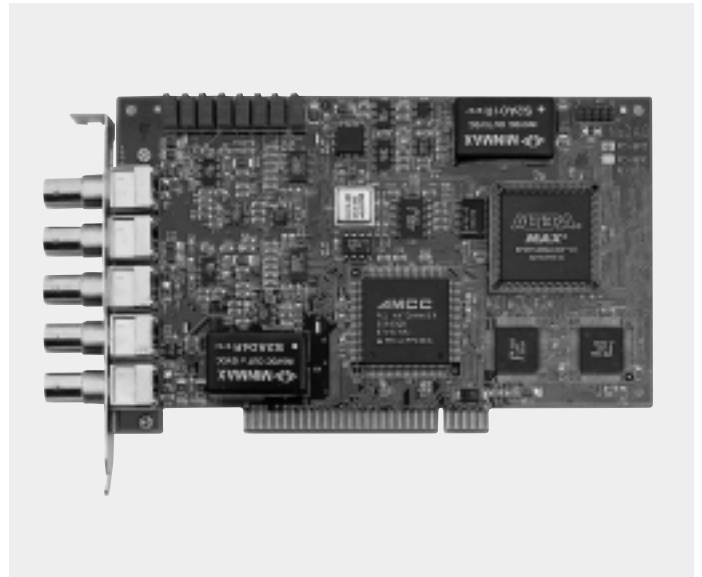


# PCI-9812/9810

## 20MHz Simultaneous 4-CH Analog Input Cards

### Features

- 32-bit PCI Bus, Plug and Play
- Up to 20 MHz sampling rate per channel
- 4 single-ended simultaneous input channels
- 12-bit (9812) or 10-bit (9810) analog input resolution
- 4 A/D converters, one converter for each analog channel
- On-board 32k words FIFO
- Bipolar signal input range (+/-5V, +/-1V)
- Five A/D trigger modes: software trigger, Pre-trigger, Post-trigger, Middle-trigger and Delay-trigger
- Bus-mastering DMA data transfer
- Programmable sampling rate
- Compact, half-sized PCB



### Introduction

#### Simultaneous 4-Channel Sampling

The PCI-9812/10 is equipped with 4 AD converters at 20MHz simultaneous sampling rate. The high speed and simple use allow the PCI-9812/9810 to serve many applications, such as image digitizing, medical applications, vibration testing equipment, and RF or base band signal digitization. The PCI-9812 card provides the best cost / performance ratio for high-end applications.

#### A/D Data Throughput

When 4 channels are starting at the same time, the total data throughput from the AD converter to the on-board FIFO memory will be 160M bytes /sec. (160MB/s = 20MHz\*4 channels\*2 bytes/channel.) The extremely high data rate is beyond the PCI-bus bandwidth. Therefore, 32K words FIFO is designed for buffering the data.

#### PCI-bus Bandwidth

The burst PCI bandwidth is 132MB /sec. However, the effective sustained data rate is usually less than 100MB/s. This value may be even lower when many PCI add-on devices are used at the same time. If the total AD data throughput is lower than the PCI bandwidth, then the AD data can put into the host memory through the Bus-mastering DMA, and the total acquiring data length could be up to 64M bytes which is the limitation of the PCI controller.

If the total AD data throughput is higher than the PCI bandwidth, then the maximum data length will be limited by the size of on-board FIFO.

#### On-board FIFO Memory

There are 32K words (32K samples) FIFO on-board. When 4 channels are used, the FIFO size is 8K samples pre channel. When two channels (#0 and #1) are used, the FIFO size is 16K samples per channel. When only one channel is used, the FIFO size is 32K samples.

#### Bus-mastering Data Transfer

PCI bus-mastering DMA is necessary for high speed DAQ in order to utilize the maximum PCI bandwidth. The bus-mastering controller built in the PCI controller controls the PCI bus when it becomes the master of the bus. Bus mastering reduces the size of on-board memory and the CPU loading because data is directly transferred to the computer's memory without host CPU intervention.

#### A/D Signal Conditioning

To control the A/D signal source, the signal type and range should be considered. The available signal input ranges for PCI-9812/10 are  $\pm 5V$  or  $\pm 1V$ . The input impedance for high speed applications should also be considered. The selectable input impedance values are 50 Ohm, 1.25 K, 15M ohm.

#### A/D Conversion Modes

The conversion mode determines the timing of conversions. There are three sources for A/D conversion timing: internal pacer clock, external sine wave or external square clock. The frequency of internal A/D pacer clock is programmable. The maximum clock rate is 20MHz. The use of external clock is more flexible because users can generate any clock frequency. The external clock must be 2 times higher than the sampling rate, for example, 36MHz external clock provide 18 MHz AD sampling rate.

#### A/D Trigger Sources and Modes

The PCI-9812/10 provides versatile trigger sources, including software trigger, external digital trigger and external analog trigger. Users can utilize the signals on any analog input channel as the trigger signal. The post-trigger, pre-trigger, middle trigger and the delay trigger can be implemented in combination with the software and hardware techniques.

## Specifications

### Analog Input (A/D)

- Max. sampling rate: 20 MHz samples/sec.(Note 1)
- Converter: B.B. ADS800 series or compatible
- Input channels: 4 single-ended
- Resolution
  - PCI-9812: 12-bit
  - PCI-9810: 10-bit
- Input range
  - Bipolar:  $\pm 1V$ , or  $\pm 5V$  (selected by soldering pads on PCB)
- Accuracy: Gain Error  $\pm 1.5\%$
- Input impedance: 50 / 1.25K / 15M  $\Omega$  (selected by soldering pads on PCB)
- FIFO Size: Total 32K samples, 8K samples per channel (Note 1)
- Trigger source: software trigger, external digital trigger and external analog threshold comparator which using internal D/A to set trigger level
- Trigger mode: Software-trigger, Pre-trigger, Post-trigger, Middle-trigger and Delay-trigger
- Data transfer mode: Bus mastering DMA only
- Clock source: Internal clock, External digital clock, External sine wave. (Note 2)
- Internal clock frequency: programmable 40 MHz / n (n=2,4,6,8..... 256)

### Digital Input

- Number of channels: 3 TTL compatible inputs with 10K Ohm pull down resistor
- Input voltage
  - Low: Min. 0V; Max. 0.8V
  - High: Min. +2.0V
- Input load
  - Low: +0.5V@ 0.2mA max..
  - High: +2.7V min.@ 20mA max..

### General Specifications

- Connector
  - 5 BNC for analog input (Channel #0~#3, external clock)
  - 9-pin header for digital input and trigger input (An accessory is used to extend the on-board header to the PC back panel.)
- Operating temperature: 0°~ 50° C
- Storage temperature: -20°~ 80° C
- Humidity: 5 ~ 85%, non-condensing
- Power consumption: +5 V @ 1.4A typical
- Dimensions: 173 mm x 108 mm

## Ordering Information

### PCI-9812

20MHz Simultaneous 4-CH 12-bit A/D card

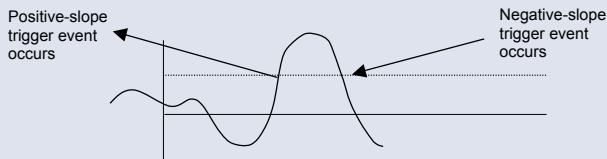
### PCI-9810

20MHz Simultaneous 4-CH 10-bit A/D card

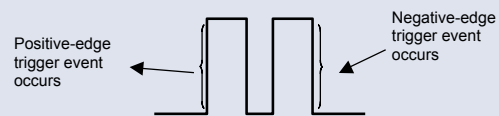
*Note 1: With a single channel enabled, the maximum sampling rate is 20 MHz. When 2 channels are enabled, the 20 MHz sampling rate can be reached only when the number of samples for each channel is less than 16k. When 4 channels are enabled, the 20 MHz sampling rate can be reached only when the number of samples for each channel is less than 8k.*

*Note 2: external clock frequency is 2 times of the AD conversion frequency. The external clock must be continuous due to the pipelined structure of the ADC.*

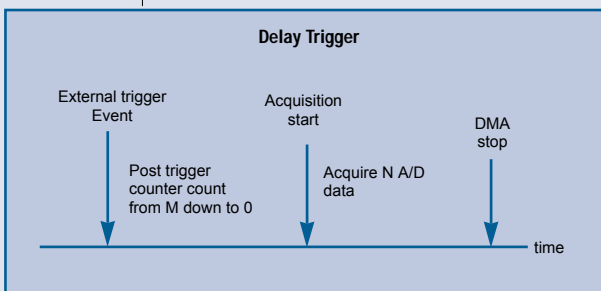
### External Analog Trigger



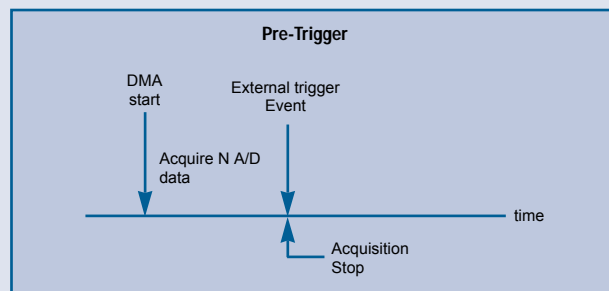
### External Digital Trigger



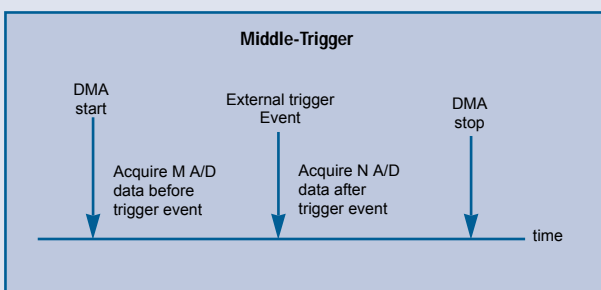
#### Delay Trigger



#### Pre-Trigger



#### Middle-Trigger



#### Post-Trigger

